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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,401	12/08/2000	James Murray	003242.P014	1880

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EXAMINER	
SCHNEIDER, JOSHUA D	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,401	MURRAY ET AL.	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,12-16,21,22,24-27 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,12-16,21,22,24-27 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 6, 12, 13, and 15, have been considered but are moot in view of the new ground(s) of rejection.

2. The Johnson reference was used to teach the termination and re-execution of a DMA transfer. Applicant has amended to include new limitations including (i) configurable system logic having programmable logic; (ii) a configurable system interconnect coupled between the configurable system logic and a DMA controller; and (iii) an input/output (I/0) device coupled to the DMA controller, wherein the I/0 device is implemented in the programmable logic and the DMA controller re-executes a DMA transfer from the beginning with the I/0 device upon receiving a retransmit request signal from the I/0 device. The Johnson reference does not explicitly teach using a configurable system interconnect coupled between the configurable system logic. The specification of the instant application teaches that the configurable system interconnect is a system bus and the configurable system logic may be used to implement device components including one or more I/O devices. The description of the configurable system logic's flexibility as a programmable logic device is often embodied by a FPGA. The new rejection that follows makes use of such an interpretation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6, and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,947,366 to Johnson in further view of U.S. Patent Application Publication 2003/0028408 to RuDusky.

5. With regards to claim 1, Johnson teaches a configurable system interconnect (column 10, line 34, through column 11, line 8), direct memory access (DMA) controller (column 2, lines 7-8), I/O devices coupled to the DMA controller (Fig. 1, element 120, and column 3, lines 4-12), and the termination of a DMA transfer before a terminal count is reached (cancellation of transfer, column 29, lines 1-65). Johnson fails to explicitly teach the I/0 device implemented in the programmable logic. RuDusky teaches that an FPGA can be used to implement a variety of system devices (paragraphs 48-55) including configurable system interconnects (paragraph 53) and I/O devices implemented in programmable logic (paragraphs 50-52). It would have been obvious to one of ordinary skill in the art a the time of invention to use the FPGA's of RuDusky as an I/0 device implemented in the programmable logic in combination with the DMA termination system of Johnson in order to create a system that allows for easy reprogramming for implements many specific designs for testing at low cost.

6. With regards to claim 6, Johnson teaches a configurable system interconnect (column 10, line 34, through column 11, line 8, Fig. 1, elements 105 and 112), coupled to the I/O device (Fig. 1, element 120, and column 3, lines 4-12) and a DMA controller (column 29, lines 1-65), a CPU coupled to the system interconnect (Fig. 1 elements 101), and a memory coupled to the system interconnect (Fig. 1, element 103, and column 3, lines 4-12). Johnson fails to explicitly teach the I/0 device implemented in the programmable logic. RuDusky teaches that an FPGA can be used to implement a variety of system devices (paragraphs 48-55) including configurable system

interconnects (paragraph 53) and I/O devices implemented in programmable logic (paragraphs 50-52). It would have been obvious to one of ordinary skill in the art a the time of invention to use the FPGA's of RuDusky as an I/0 device implemented in the programmable logic in combination with the DMA termination system of Johnson in order to create a system that allows for easy reprogramming for implements many specific designs for testing at low cost

7. With regards to claim 24, Johnson teaches a first channel coupled to the I/O device to facilitate the transfer of data (column 29, lines 32-42).

8. With regards to claim 25, Johnson teaches memory means to store configuration data (column 29, lines 32-42).

9. With regards to claim 26, Johnson teaches error-checking logic for checking data transfers for errors (column 29, lines 1-65).

10. With regards to claim 27, Johnson teaches control logic to control the transfer of the data (column 29, lines 32-42).

11. Claims 2, 12-16, 21, 22, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,947,366 to Johnson as applied to claims 1, 6, and 24-27 above, and further in view of U.S. Patent 6,298,396 to Loyer et al.

12. With regards to claim 2, Johnson teaches the re-execution of a data transfer (column 29, lines 32-42) with an I/O device, but fails to explicitly teach the re-execution of a DMA transfer. Loyer teaches that it was well known in the art at the time of invention to restart the transfer from the beginning of the packet in order to prevent the loss of the packet data (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55). The error signals from the receiving device act to terminate the current DMA transfer and request a

retransmit of the packet. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA error handling of Loyer with the DMA cancellation of Johnson in order to create a system that transfers data with a minimal amount of data having to be retransmitted for error recovery.

13. With regards to claim 12, Johnson teaches a configurable system interconnect (column 10, line 34, through column 11, line 8), a direct memory access (DMA) controller (Fig. 1, element 120, and column 3, lines 4-12), and an I/O devices coupled to the DMA controller (Fig. 1, element 120, and column 3, lines 4-12), but fails to explicitly teach the re-executing of a DMA transfer from the beginning upon the receiving of a request signal and the I/0 device implemented in the programmable logic. RuDusky teaches that an FPGA can be used to implement a variety of system devices (paragraphs 48-55) including configurable system interconnects (paragraph 53) and I/O devices implemented in programmable logic (paragraphs 50-52). It would have been obvious to one of ordinary skill in the art a the time of invention to use the FPGA's of RuDusky as an I/0 device implemented in the programmable logic in combination with the DMA termination system of Johnson in order to create a system that allows for easy reprogramming for implements many specific designs for testing at low cost. Loyer teaches that it was well known in the art at the time of invention to restart the transfer from the beginning of the packet in order to prevent the loss of the packet data (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55). The error signals from the receiving device act to terminate the current DMA transfer and request a retransmit of the packet. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA error handling of Loyer with the DMA cancellation of

Johnson in order to create a system that transfers data with a minimal amount of data having to be retransmitted for error recovery.

14. With regards to claims 13 and 15, Johnson teaches a configurable system interconnect (column 10, line 34, through column 11, line 8), a direct memory access (DMA) controller to transfer data between and first and second device (column 2, lines 7-8), I/O devices coupled to the DMA controller (Fig. 1, element 120, and column 3, lines 4-12), and the re-executing of a DMA transfer from the beginning upon the receiving of a request signal (column 29, lines 32-42). Johnson teaches the termination of a DMA transfer (column 29, lines 1-65) with an I/O device. Johnson teaches the use of acknowledge signals in DMA transfers (column 9, lines 37-50, and column 10, lines 12-17). Johnson teaches the erasing by reloading the configuration registers with control information (column 29, lines 32-42). Johnson fails to explicitly teach the I/0 device implemented in the programmable logic. RuDusky teaches that an FPGA can be used to implement a variety of system devices (paragraphs 48-55) including configurable system interconnects (paragraph 53) and I/O devices implemented in programmable logic (paragraphs 50-52). It would have been obvious to one of ordinary skill in the art a the time of invention to use the FPGA's of RuDusky as an I/0 device implemented in the programmable logic in combination with the DMA termination system of Johnson in order to create a system that allows for easy reprogramming for implements many specific designs for testing at low cost. Johnson fails to explicitly teach the re-execution of a DMA transfer (column 29, lines 32-42) with an I/O device. Loyer teaches that it was well known in the art at the time of invention to restart the transfer from the beginning of the packet in order to prevent the loss of the packet data (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55).

The error signals from the receiving device act to terminate the current DMA transfer and request a retransmit of the packet. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA error handling of Loyer with the DMA cancellation of Johnson and RuDusky in order to create a system that transfers data with a minimal amount of data having to be retransmitted for error recovery.

15. With regards to claim 14, Johnson teaches the erasing by reloading the configuration registers with control information (column 29, lines 32-42).

16. With regards to claim 16, Johnson teaches the reloading the configuration registers with control information (column 29, lines 32-42). Loyer also teaches that it was well known in the art at the time of invention to restart the transfer by reloading the registers with the control information, thereby clearing the counter of the previous transfer (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55).

17. With regards to claim 21, Loyer teaches that it was well known in the art at the time of invention to restart the transfer from the beginning of the packet in order to prevent the loss of the packet data (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55). The error signals from the receiving device act to terminate the current DMA transfer and request a retransmit of the packet. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA error handling of Loyer with the DMA cancellation of Johnson and RuDusky in order to create a system that transfers data with a minimal amount of data having to be retransmitted for error recovery. The associated requests for the restarting of these transfers are inherent. After an error, the use of acknowledge

signals will again be needed, as they are part of the basic transfer signaling used in all of the DMA accesses (Johnson, column 9, lines 37-50, and column 10, lines 12-17).

18. With regards to claim 22, Loyer teaches that it was well known in the art at the time of invention to restart the transfer from the beginning of the packet in order to prevent the loss of the packet data (column 11, line 55, through column 12, line 21, and column 13, line 35, through column 15, line 55). The error signals from the receiving device act to terminate the current DMA transfer and request a retransmit of the packet. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA error handling of Loyer with the DMA cancellation of Johnson and RuDusky in order to create a system that transfers data with a minimal amount of data having to be retransmitted for error recovery. The associated requests for the termination and restarts of these transfers are inherent. After an error, the use of acknowledge signals will again be needed, as they are part of the basic transfer signaling used in all of the DMA accesses (Johnson, column 9, lines 37-50, and column 10, lines 12-17).

19. With regards to claim 29, Johnson teaches a first channel coupled to the I/O device to facilitate the transfer of data (column 29, lines 32-42).

20. With regards to claim 30, Johnson teaches memory means to store configuration data (column 29, lines 32-42).

21. With regards to claim 31, Johnson teaches error-checking logic for checking data transfers for errors (column 29, lines 1-65).

22. With regards to claim 32, Johnson teaches control logic to control the transfer of the data (column 29, lines 32-42).

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDS

KIM HUYNH
PRIMARY EXAMINER

11/28/05